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Wafer-scale integration brings low cost and a small footprint to active antenna arrays

Fabricating a 256-element steerable antenna array on an eight-inch wafer is quite a feat, given the multitude of issues—steering the antenna, optimizing the RF paths and the like. By addressing these and other matters, one at a time, it becomes clear that realization is well within reach.

By Fred Mohamadi

Tremendous interest is developing with regard to the use of Si-substrate technology for SHF, RF and microwave applications. Wafer scale integration using Si substrate makes it possible to fabricate cell array units in a module that comprise antenna and RF circuitry for beam-forming applications [1-3]. These technologies will, in turn, make possible the deployment of low-cost, steerable arrays for military and commercial applications.

However, there are a number of challenges in the design and fabrication of such arrays. They include the fabrication of Si-based substrate RF blocks and the distribution of RF signals to each element. Then there are issues such as the impact of signal attenuation and crosstalk, the accuracy required in phase resolution, and beam-width management. Finally, there are the questions of noise cancellation, dc signal distribution, and the control capability of beam forming for tracking and beam steering.

We will address these various issues and provide a number of suggestions for dealing with them.

Getting acquainted with the wafer scale module

The wafer scale array module (WSAM) described here provides transmit and receive functions at a bandwidth of 5%. The module is designed to scan ±30 degrees at a 3 dB drop-off from maximum-emitted radiated power (ERP). In one possible scenario the module would deliver 10 W to 40 W ERP broadside to the WSAM—assuming the module is operating at 3.3 V.

The WSAM consists of a 16 by 16 element antenna and its associated electronic circuitry. The total number of elements is 256. Fabricated on an 8-inch (200 mm) CMOS or Si-Ge wafer, the antenna elements are spaced 8 mm apart.

Figure 1. Maximum number of elements vs. antenna element pitch.

Figure 2. Antenna array element RF module for Tx/Rx functions and controller’s local management functions.
instance, an eight-inch wafer can be used for 64-element array with 15 mm pitch (separation plus antenna size) corresponding to a 10 GHz RF signal. Alternatively, a 1024-element array operating at 40 GHz could be built on an eight-inch wafer substrate. This would maximize the gain of the antenna array.

As for the array architecture, the WSAM uses a so-called “tile” array configuration in which the radiating element layer and the signal distribution layer are parallel to each other. The radiating element layer can be either a CMOS or a Si-Ge RF device layer. The layers are interconnected using a special manufacturing process discussed later in this article. A block diagram of the WSAM is shown in Figure 2 and the module’s form factor is illustrated in Figure 3.

With regard to the RF portion of the module, it consists of a 256-network line RF signal divider. In our example a 2-micron-thick, metal layer 5 is used. Included in each cell are a low noise amplifier (LNA), a programmable power amplifier (PA), and analog switches to select Rx or Tx modes, an attenuator, and a phase shifter unit, as well as a controller.

Managing the module

The WSAM must communicate with an external electronic unit (baseband and MAC functions). Here is where the mixed signal-based controller plays a number of important roles. It addresses power management based on a peak detection mechanism at the receiver. There is a PA gain control to optimize efficiency, pre-distortion capability to address linearity, and a LNA gain control to optimize SNR performance. The controller also operates a 3-bit, digitally controlled phase shifter. The controller plays additional roles, for there is an optional field to address LNA gain control, and Tx or Rx switch selection. Finally, there is a power management function to address sleep mode operation.

As for power distribution, the necessary regulated and selected bias voltages are fed to the gate and drain of the PA, to the LNA, the analog switches, the phase shifter, attenuator circuit, and controller unit.

The wafer scale integration concept is illustrated in Figure 3. The module comprises three main layers—a radiating element layer, a device layer and a signal distribution layer. The radiating element layer can consist of 256 microstrip patches, or dipole, elements. To provide low resistance thermal paths that ensure effective heat dissipation, a layer of heat-conducting material can be used to coat the active device side of the wafer.

An important consideration is the maximum allowable current density of 10⁶ amperes/cm², as governed by the electromigration design rules. This sets an upper limit of 2 mA per micron length for a 2+-micron-thick Al-Cu line. The RF interconnection layer consists of coplanar waveguide (CPW) or shielded microstrip transmission lines and distributed signal reshapers and repeaters.

If we look at the performance of the isolated antenna elements, here are some typical specifications. In one application, an isolated element provides a bandwidth of 5% for a 2:1 VSWR at 7 dB gain. The element is excited through a metal rod connected to a via that is filled with a deposited metal layer. After proper phase shifting, the element connects to an output of an analog RF switch powered by a PA. Similarly, in receive mode, this element can deliver collected radiation to the input of the RF switch feeding the LNA, before properly phase shifting it.

As for the power amplifier, it could be a three-stage, 50-micrometer to 200-micrometer, gate-width amplifier that delivers 200 mW at 20 dB gain and 25% efficiency. The phase shifter provides at least three bits of switched line lengths with 3 degrees rms maximum variation. The phase-shifting device has less than 5 dB insertion loss (ideally below 1 dB) at room temperature. The RF switches, LNA, PA, phase shifter and the controller are all included in the die. Once it has been adequately shielding and thereby isolated to prevent electromagnetic coupling to active devices, the die fits under the antenna plate.
WSAM, we can go on to examine the fabrication steps, in detail.

**Wafer scale integration using a Si-substrate**

The proposed WSAM implementation is shown in Figure 4.

1. Prior to any standard process step, a heavily doped, deep conductive junction is formed as a contact junction for the antenna feed. This is similar to a deep-diffusion junction process employed in the manufacture of double-diffused or triple-diffused CMOS (DMOS) high-voltage devices. The deep junction is used to separate, and thereby effectively isolate the antenna feed lines from the active devices—which are the LNA, the phase shifter and the PA. This junction also provides a low-resistance, signal-path region that is essential for minimizing insertion loss to the antenna plates, patch or dipole. The deep junctions will be accessed through the backside of the wafer. The antenna plates will then be fabricated.

2. The active devices are manufactured using standard Si-substrate, CMOS or Si-Ge processes.

3. Passivation of the active devices is accomplished by first applying a low-temperature, deposited porous silica SiOx. Then a thin layer of Nitridized oxide (SixOyNz) is applied as the final layer of passivation. Thickness of the sealing layer is a fraction to a few micrometers.

4. The top layer of the active devices is coated with a thermally conductive material, taped to a plastic adhesive holder, and then flipped to expose the unprocessed side of the wafer.
5. The wafer thickness is then reduced by grinding the backside of the wafer to a thin layer, no more than a few hundreds of a micrometer thick.

6. An additional layer of metalization is sputtered, evaporated, deposited, or alternatively coated using conductive paints. This layer forms a reflective plane for directivity and shields the active devices from antenna radiation. It also provides contact fillers to the heavily doped Si that connects to the feed lines of the antenna patch or dipole layers. The deposited material at the backside of the wafer is patterned as metal lumps on top of the highly doped Si contact-to-antenna feed circuitry. These metal lumps ease the penetration of via rods that will form Ohmic contacts with the feed circuitry and connect to the antenna plates, thereby preventing cracking of the Si substrate.

7. The target alignment patterns that were
Figure 10. Antenna array with distributed amplifiers, array and RF feed lines in two different paths.

Etched during the normal manufacturing process of the silicon wafer are then used to precisely locate the vias—the metal layer that connects the antenna to the feed lines in the Si substrate. This process can use an infrared alignment scheme, as is frequently employed in the manufacture of some MEMs devices.

8. A layer of porous material, or honeycomb structure, separates the antenna layer from the shield and Si substrate. This material has a low dielectric constant so that it effectively decouples the antenna from the substrate, thereby ensuring satisfactory antenna efficiency.

9. A top plate of thin Teflon or a similar material with a low dielectric constant is used as a substrate for the antenna plates. As an option, a very thin layer of high dielectric material, such as Ta$_2$O$_5$, can be used to reduce horizontal surface waves.

10. Dipole or patch patterns, as well as alignment patterns, are defined in the deposited metal layers on top of the Teflon layer.

11. Precision rods are inserted to form through-hole contacts and to complete the antenna-to-feed electrical connections. Alternatively, the vias can be precision drilled and filled with conductive material to form highly Ohmic contacts.

12. A final passivation layer is applied on top of the antenna layers to provide impedance matching to free space and to protect the devices.

13. The connectors to the RF Rx/Tx unit and controller are then brought up to the external area for beam steering/tracking.
and for the signal processing associated with the beam-forming algorithms.

14. Finally, the finished wafer is flipped and the RF connectors are attached.

There are, of course, alternative manufacturing processes and one is shown in Figure 5. Here the deep conductive junctions are formed from the backside of the wafer and then the front side devices are fabricated with the standard semiconductor manufacturing process previously described. The rest of the process is also identical to the previously mentioned manufacturing flow. Shown in Figure 5 is an alternative implementation of the cell antenna that uses a dipole antenna.

Signal distribution limitations and proposed solutions

It turns out that the limitations imposed by the metal routing, so essential for high-density and high-speed semiconductor products, have been a subject of study for decades\(^4\). Another hindrance to performance is the low-resistivity substrate, used to improve yields and suppress latch-up. Nonetheless, such substrates contribute significant, high-frequency losses. So it is no surprise that the silicon substrate has been the major limitation in X-, K- and Q-band applications. Fortunately, the current trend of metal
technology scaling alleviates this concern, as illustrated in Figure 6.

As depicted in Figure 6b, the bottom metal layers scale to smaller pitches to enable denser routing. Whereas the top metal layers scale to larger pitches to enable thicker lines for improved power and high-frequency RF handling—as well as a lower global routing loss. The interlayer dielectric thickness is almost twice the metal thickness. This minimizes interlevel shorts and reduces capacitance. As a result, the top metal layers are situated further away from the silicon substrate, thereby reducing the losses associated with the substrate. At present, the current trend is for the distance from the top-level metal to the silicon substrate to be approximately 1.5-micrometers per metal layer.

Let us look next at the effects of line width and associated skin depth. The impact of skin depth on signal attenuation has been modeled to address the resistance of metal lines as a function of frequency of the signal[5-10]. Shown in Figure 7a is the impact upon the S-parameters of coplanar waveguides fabricated with 2-μm thick, aluminum metalization. To demonstrate the impact of insertion loss and line resistance as a function of frequency, a top layer has been used. The results indicate that feed line signal attenuation is serious, as seen in Figure 7b. In fact, for a 256-element active antenna cell, power deterioration is -48 dB. Also quite pronounced is the impact of capacitive coupling to the substrate and inductive coupling to the ground lines. The insertion loss worsens from -5 dB to -10 dB for a 5-mm length line with various trace widths and spacings, as denoted in Figure 7a. It should also be noted that for a WSAM, which must feed 256 active cells, the signal-distribution line loss remains significant for line lengths up to approximately 100 mm.

Minimizing jitter

The control of jitter by removing intersymbol interference (ISI) and crosstalk is an important part of any proposed integration scheme because the jitter issue is a critical factor in meeting the required bit error rate (BER) in most digital communication applications. However, the issue is less important in radar applications where a reflected continuous wave signal is used to calculate the distance and velocity of an object.

Precision timing deterioration and random phase shift, cause significant jitter in the delivered signal. By far, this has the worst impact on beam forming. This means that increments of phase shift need to be accurately managed in each cell—to better than $2^\circ$ to $3^\circ$ rms per available phase increment.

One way to reduce jitter is to employ re-timing circuitry. However, the use of a PLL-based re-timer in each cell results in more complexity in circuit design and also demands very high bandwidth processes—such as IBM’s 8HP, or even its 9HP process technology. Despite the precision phase management that can be achieved with PLL in the RF signal paths, its use can introduce design risks. What’s more, it can lead to excess power consumption, given the high data rates that must be employed.

To further address jitter management, future designs may use a PLL-based, re-timer with each split section. As shown in Figure 8 the line interweaving minimizes jitter whereas the distributed amplifiers behave as signal boosters, thereby compensating for the resistive line loss.

The signal-carrying RF lines need to be combined or recombined at each split.
These steps can be accomplished by employing RF signal repeaters that are realized with distributed amplifiers, as depicted in Figure 8. The RF signal is reshaped to compensate for the line loss, replacing the traditional Wilkinson-type combiners and decombiners in combination with distributed amplifiers.

This methodology splits each of the wide, RF-carrying line into multiple, thinner lines so that each can be optimized, thereby make a minimal contribution to the net resistance. This is essential because the effective current density is three to five times the skin depth. The combining takes advantage of distributed amplifiers that provide sufficient bandwidth to compensate for the insertion loss. When compared with current passive combiners, the enhancement realized with this approach is substantial.

The concept of RF signal delivery to each cell, including the branching (splitting) junctions is illustrated in Figure 9. The dc and control lines are distributed in a similar routing direction. However, they use all metal layers—metal layers 1 to 5—so that the isolation realized with the low Ohmic grounds can be managed. An enhancement to the proposed approach would be to design a voltage regulator at each splitter/branching so that ripple effects and noise accumulation on the dc power lines would be minimized.

The concept of including distributed amplifiers and active combiner/decombiner blocks for RF paths at each splitting junction, colored in blue, is depicted in Figure 10. Similarly, dc supply enhancements can be addressed by including a band-gap voltage regulator. Also, a large supply-to-ground distributed capacitor could be connected in parallel to filter out high-frequency noise.

For a three-bit shifter, phase shift increments are eight discrete phases: -180, -135, -90, -45, 0, 45, 90, 135, 180 (same as -180). In this case, the incremental phase is 3.0 picoseconds for a 40 GHz bitstream. In order to assure a 70% eye opening for satisfactory signal detection, the maximum tolerable total jitter must be less than 1 picosecond. As a result, the total jitter limitation, including rise and fall time on the precise location of the beam, the signal-to-noise (SNR) of the RF data path, and the active circuitry must be less than 1 picosecond. Based upon an initial evaluation illustrated in Figure 11, it can be concluded that for a phase error rate of better than 10⁻³ and a SNR of better than 20 dB, the maximum tolerable jitter noise in the feed system must be less than 15 dBm.

Shown in Figure 12 is a simulation for a 16-element, sub-array radiation that uses the implementations previously described. The gain of the sub-array is 3 dB to 4 dB less than the maximum attainable as a result of spacing the elements at slightly less than a half-wavelength apart. However, this compromise enables the implementation of 256 active antenna cells on a WSAM.

Conclusion

As we have discussed, attenuation of the RF signal and jitter deterioration, as a result of crosstalk and ISI, are the key areas of focus for an optimized design of a WSAM. Distributed amplifiers, spatial phase balancing and crosstalk cancellation are also crucial to improve the signal-to-noise ratio of the delivered RF signal to the active antenna elements. In the future, advanced CMOS and Si-Ge processes will enable the use of adaptive equalization at the antenna-element receiver, at the retimers.
and at the corporate-feed split points to enhance signal quality and thereby provide ultratight control of jitter. And as we have explained, jitter management is crucial for proper phase-shifter management. RFD

References


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