

# Frequency divider design strategies

Typically, in frequency divider design, the trade offs are around the maximum operating frequency, power consumption, number of transistors needed and flexibility. Depending on the specific application the frequency divider is used, analog or digital approaches may be adopted. This paper will cover the fundamentals of both approaches.

By Louis Fan Fei

The frequency divider is an important building block in today's RFIC and microwave circuits because it is an integral part of the phase-locked loop (PLL) circuit. In a typical PLL loop, the output of the voltage-controlled oscillator (VCO) is divided down by the frequency divider to a frequency the temperature-compensated crystal oscillator (TCXO) operates (typically from 10 MHz to 30 MHz). The divided signal and TCXO are fed into the phase detector for comparison. The output phase difference is used to adjust the VCO output frequency. The frequency divider is also widely used to generate a precision I/Q signal if the input signal has a 50% duty cycle, for the modern in-phase and quadrature (I/Q) modulator or demodulator. For the signal with duty cycle other than 50%, an additional divide-by-2 can be used to generate the 50% duty cycle. Compared with the traditional resistor and capacitor (RC) quadrature generation, the frequency divider approach is easier to implement, is lower power and offers smaller phase imbalance.

## Digital logic approaches

Since the PLL is part of the RF circuit, one would think the frequency divider should be analyzed by the analog circuit theory. But it turns out the most widely used approach is based on the digital logic gate. The RF analog engineer typically puts on the digital logic hat for a minute when analyzing the frequency divider. It will be much easier to understand and analyze the digital approach in the digital domain and the analog approach in the analog domain. Within the digital domain, the design strategy can be further divided into two categories: static logic and dynamic logic.

The static implementation is the most popular approach. The memory cell is a true bistable circuit, unlike the parasitic capacitor used in the dynamic approach. One standard design is the divider by 2 cell shown in Figure 1. In today's design software, it is treated as a standard digital cell. There are many names for circuits similar to Figure 1, such as a Johnson divider, toggle switch, complementary metal oxide semiconductor (CMOS) prescaler, emitter couple logic (ECL) and a source couple logic (SCL). When it is implemented in CMOS, it is called SCL. When it is implemented in a bipolar process, it is logically called ECL. For this illustration, CMOS implementation (SCL) is used.

The first look at this design might be intimidating for an RF design engineer. It doesn't look like an RF circuit with the exception of the differential amplifier and cross-coupled negative channel field effect transistor (nFET) of a VCO. Treating it as a pure RF circuit will make it much harder to understand. However, once analyzed in the digital domain, the answer will be clear. Before the detailed discussion of this circuit, some of the fundamental digital logic theory should be reviewed. Shown in Figure 2 is a logic gate for the toggle switch. The theory of operation is straightforward. It is essentially an edge-triggered master/slave D flip-flop (DFF). The inverted output is fed

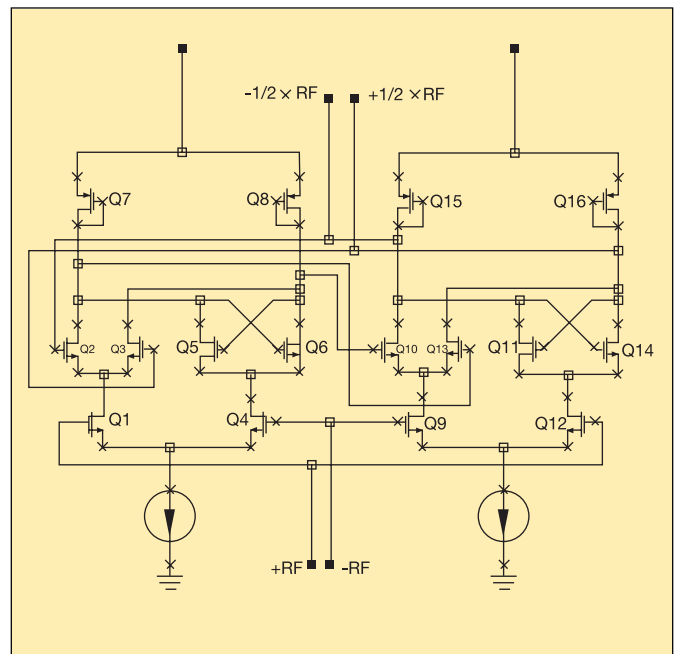


Figure 1. Divide-by-2 SCL.

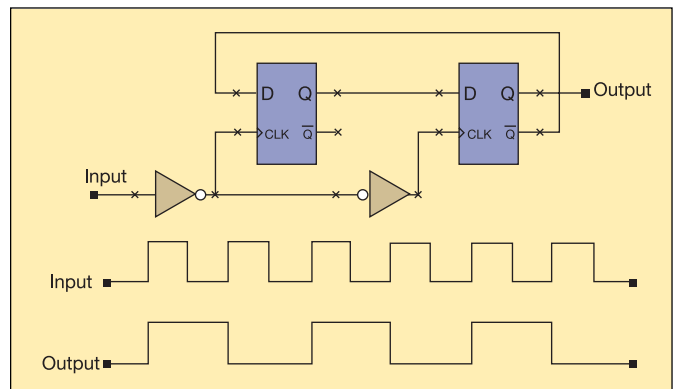


Figure 2. Logic diagram of toggle switch.

back to the input port D. The same clock is used to drive both level-triggered DFF with opposite logic. The reason for the inverter is to make an edge-triggered DFF out of the two level-triggered DFF. The first DFF is commonly called the master DFF and the second one is normally referred to as the slave DFF. Either master DFF or slave DFF is activated in each clock cycle, not both DFF at the same time

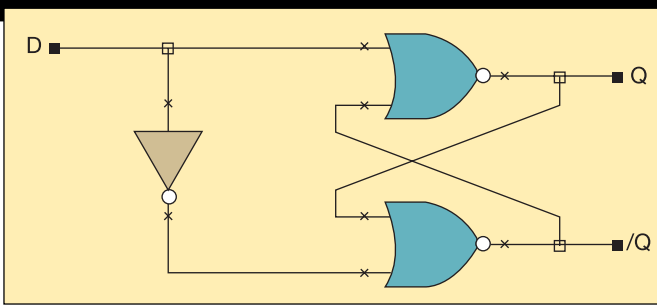


Figure 3. DFF at logic gate level.

(because of the inverter between them). As shown in Figure 2, each positive input clock cycle is loaded into the DFF. On the next cycle, inverted output again is fed back to the input, which causes the output to toggle. It is why toggle DFF is a more descriptive name for this circuit. The same event repeats for every two input clock cycle. Thus, output frequency is half of the input frequency.

Comparing Figure 1 and Figure 2, intuitively you should guess the left half of Figure 1, from Q1 to Q8, is the master DFF while the right half of Figure 2 is the slave DFF. The guess is indeed true. Zoom into the DFF—a typical DFF implementation is comprised of cross-coupled NOR gates as shown in Figure 3. Without the inverter, it is recognizable as the familiar SR latch. The next logic step is to take a look at how the SR latch logic is implemented on the transistor level. The SR latch transistor implementation is shown in Figure 4. Transistor Q2, Q5, Q7 and Q9 form the first NOR gate while Q3, Q6, Q8 and Q10 complete the second NOR gate. It should be obvious that Q2 and Q5 are the pull-down network (PDN) for passing logic 1s and Q7 and Q9 are the pull-up network (PUN) for passing logic 0s. Similarly, the pairs (Q3, Q6) and (Q10, Q8) are the counterparts for the second NOR gate. Now comparing the circuit in Figure 4 and Figure 1, the circuit in Figure 4 is the same circuit used for the edge-triggered DFF SCL implementation with minor modifications. Q2, Q5, Q3 and Q6 are still the same circuit elements rearranged slightly. Q7 and Q8 are still the active loads. Q1 and Q4 act as the input buffer. They also provide the enable function. As discussed earlier, in edge-triggered master-slave DFF, only one DFF is activated at the time. The inverter can be easily implemented by swapping the position of the “+RF” and “-RF” when feeding different DFFs.

Looking back from Figure 1 to Figure 4, we have looked at the divide-by-2 circuit at the block level (Figure 2) logic gate level (Figure 3) and transistor level (Figure 4). Figure 1 is essentially the transistor level implementation of the Figure 2. Of course, some modifications are added to complete this SCL design.

The key building block in the frequency divider is the bistable block. For the circuit in Figure 1, SR logic gate is the bistable element. However, this is not the only implementation. Another implementation is to use two inverters back to back in a feedback network as used in the memory circuit. It tends to be slower than the SCL logic.

### Dynamic DFF implementation

In dynamic DFF implementation, there is no dedicated bistable circuitry. The parasitic cap between the node acts as the storage element. It is typically called Clocked CMOS (C<sup>2</sup>MOS). One such circuit is shown in Figure 5.

This circuit uses a far less number of transistors. The theory of operation is simple. Transistors Q1 to Q4 complete essentially a tri-state inverter (INV1). Transistors Q5 to Q9 (INV2) form another inverter. The capacitor in the middle is a model for the parasitic capacitance between the gate. The capacitor's responsibility is to store the signal. Q9 and Q10 make a simple CMOS inverter to complete the feedback path needed for the toggle latch. In the positive clock cycle (RF+), INV1 is on and INV2 is off, so the signal is clocked into the storage capacitor. In the negative clock cycle (RF-), INV1 is off and INV2 is on, the signal is clocked out. There

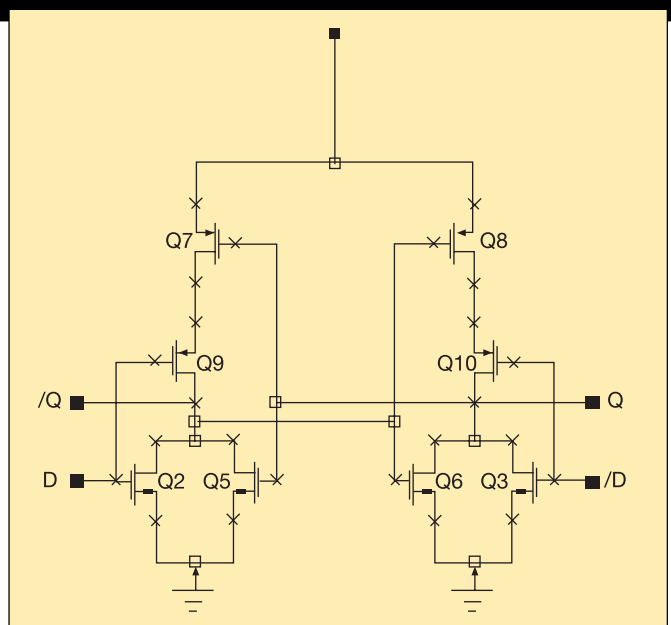


Figure 4. DFF at transistor level.

are many different flavors using a similar theory of operation.

The circuit in Figure 5 requires the complementary clock input (RF+ and RF-). Sometimes, it is more desirable to drive the frequency divider single ended. The type of logic is called true single-phase clocked (TSPC) logic. It is built on the basic C<sup>2</sup>MOS. It eliminates the differential drive requirement at the expense of more transistors. One such circuit is shown in Figure 6.

Transistors Q1 to Q6 form the master latches. Transistors Q7 to Q12 form the slave latches. Q13 and Q14 are simply the inverter to complete the feedback path needed in the toggle latch. The master latch is sometimes called double NC<sup>2</sup>MOS because two NFETs are needed in the PDN. Similarly, the slave latch is sometimes referred to as the double PC<sup>2</sup>MOS because two PFETs are needed in the PUN. When the clock is high, the master latch is activated while the slave latch is off. The opposite is true when the clock is low. The circuit shown in Figure 6 is the most basic form. There are more variations and clever designs used to reduce the number of the transistors.

Comparing the static and dynamic implementation, static logic is

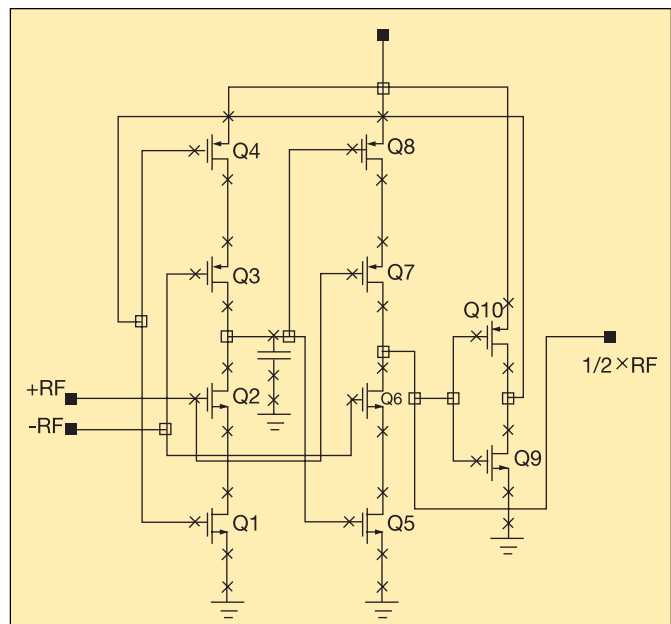


Figure 5. Dynamic DFF implementation.

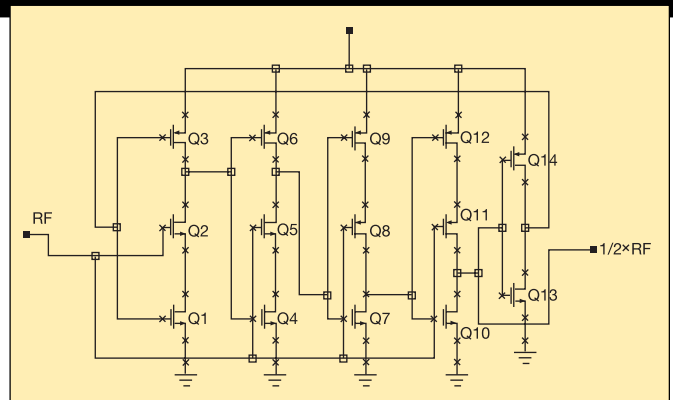


Figure 6. TSPC frequency divider.

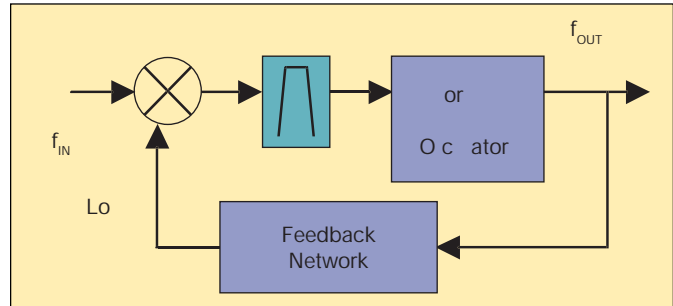


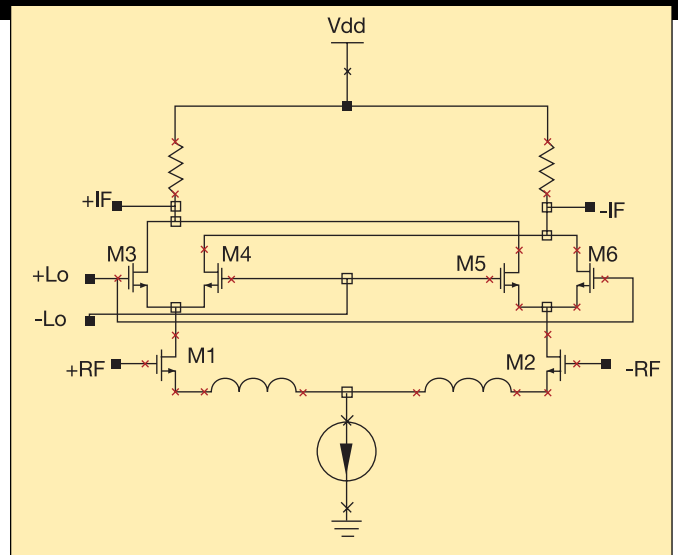
Figure 7. ILFD architecture.

faster and more reliable. The dynamic logic uses a far fewer number of transistors and is easier to implement. However, it is slow and it could consume more power because full CMOS swing is needed in certain applications.

### Analog approach

The frequency divider with analog approach is also widely used. It tends to be used in the very high frequency millimeter wave range, anywhere from 20 GHz up to 100 GHz. Also, they tend to be in discrete form. The reason for this is the CMOS or BiCMOS process still doesn't have high enough operating frequency range as the more exotic process like pHEMT or heterojunction bipolar transistor (HBT). The analog approach is often called regenerative injection-locked frequency divider (ILFD). Recently, there has been a lot of research to use this technique with CMOS at much lower operating range. However, operating bandwidth is fairly narrow due to the nature of this architecture. In VCO design, one of the key parameters is VCO pulling. Basically, the VCO output frequency will be pulled away if a continuous wave (CW) signal at a different frequency is nearby. VCO pulling is an undesired characteristic, but it is used cleverly to design the ILFD. ILFD is built on this phenomenon by adding a feedback loop, along with a mixer, oscillator or an amplifier with appropriate feedback network and appropriate filters. The basic architecture of ILFD is shown in Figure 7.

From the basic mixer theory,  $f_{out} = f_{in} - Lo$ . If  $f_{out} = Lo$ , then  $f_{in} = 2 * f_{out}$ . Thus,  $f_{in}$  is divided down by half. The active device like an amplifier or a ring oscillator is needed to sustain the oscillation. The ILFD can be treated as an oscillator operating at  $f_{out}$ . The difference is ILFD's output will closely track the input. A good ILFD only oscillates when there is signal injected at the input. The filter is needed to reject all the undesired spurious signals out of the mixer. Otherwise, the ILFD could lock into an undesired frequency output. Since the physical mixer is a non-linear device, it could generate signals at  $Lo$  and its harmonics. By carefully controlling which harmonic is generated, higher divider ratio can be achieved. For example, if the  $Lo$ 's third harmonic is used, then  $Lo = 3 * f_o$ . Then  $f_{in} = 3 * f_o + f_o$ . Thus, the  $f_{in} = 4 * f_o$ , a divide-by-4 circuit is accomplished. In an ILFD design, most of the building blocks in a typical

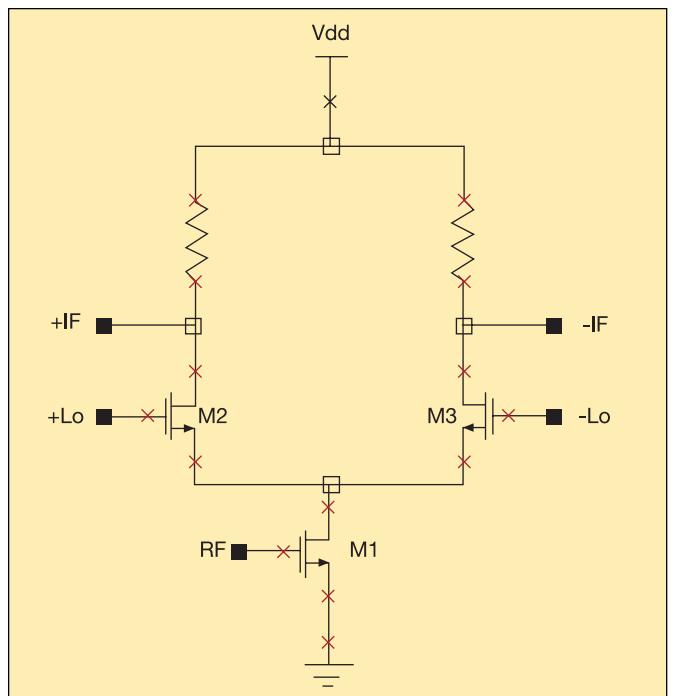


**Figure 8. Gilbert cell DBM.**

receiver are used. Filter, amplifier, oscillator, mixer and feedback network are all rich in theory. There are many good references to cover those topics in details. Some of the references are listed in the reference section. One additional comment with ILFD is on the mixer topology. In the mixer design, harmonics are undesired features. However, as illustrated, the harmonics of the mixer are used to the designer's advantage to design a good ILFD. In the active RFIC mixer implementation, a Gilbert cell double balanced mixer (DBM) is widely used. One such circuit is shown in Figure 8. A well-designed DBM will suppress the even harmonics of the Lo. Then only even divide ratio ILFD can be designed. To design an odd divide ratio ILFD, the even harmonics of the mixer is actually a desired feature. Therefore, a simpler single balanced mixer (SBM) can be used to add more flexibility. One SBM topology is shown in Figure 9.

## Summary

The frequency divider is an interesting and indispensable building block in RF or microwave circuits. There are two main design



**Figure 9. Single balanced mixer.**

approaches: digital logic and analog using injection-lock techniques. The digital logic approach can be further divided as the static DFF and dynamic DFF. Like any other receiver design, design trade offs required depend on the application. In applications from around 40 GHz to 100 GHz, an ILFD is a suitable approach because today's standard CMOS process still doesn't have the bandwidth in that range. From 10 GHz to 40 GHz, successful SCL-type frequency dividers have been reported. The power

consumption, cost and physical size need to be thoroughly compared to decide if the digital or the analog approach is used. From low GHz to 10 GHz, digital SCL is the working horse in this range. Below the low GHz frequency, a case can be made to use dynamic DFF to reduce the number of the transistors needed, thus the cost and power consumption is reduced as well. In today's RFIC, a programmable divider is often required. The digital approach offers the flexibility and modularity ILFD can't match.

The frequency divider is an actively researched area. There are more clever topologies to be discovered to reduce the size, power consumption, complexity and cost. RFD

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